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PROGRAMS AND REQUIREMENTS FORECAST FOR ARMY MISSILE MICROELECTRONIC RESEARCH, DEVELOPMENT AND MANUFACTURING METHODS AND TECHNOLOGY

ARMY MISSILE RESEARCH, DEVELOPMENT AND ENGINEERING LABORATORY, REDSTONE ARSENAL, ALABAMA

20 OCTOBER 1976

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This report contains a forecast of microelectronic technology which will be required for Army Missile during the next five years. The program and project required to achieve the required technology is defined in the work area of Research and Development or Manufacturing Technology. One section of this report is devoted to a discussion of the selection criteria used for the selection of the Manufacturing Technology program.

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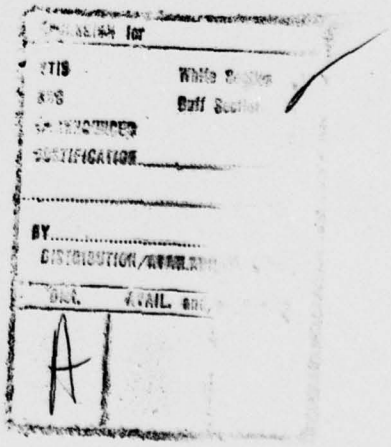

I. INTRODUCTION

The field of electronics has been in a rapid state of change for the past two decades. The invention of the transistor in 1946 launched a seemingly unending drive toward miniaturization of electronic systems and has created the new field of microelectronics. With the physical size of electronic circuits shrinking by more than an order of magnitude every five years, there has been a corresponding increase in microcircuit complexity and great improvements in system reliability.

The various technologies which have evolved and are still under development for fabricating microelectronic systems differ greatly in fabrication procedures and in performance. Yet, each of the major technologies offers certain advantages which have made it superior and successful in the particular applications which are appropriate for that technology. This report will consider in detail the following approaches: hybrid thick film, hybrid thin film, monolithic metal oxide semiconductor (MOS), monolithic bipolar (both linear and digital) and electro-optics. An attempt will be made to identify the strengths and weaknesses of each of these approaches in the light of the US Army Missile Command (MICOM) mission objectives. Particular consideration will be given to reliability, flexibility, resistance to stress, minimization of power consumption and size, and the impact of computer-aided-design. An assessment of current technology trends will be made to serve as an estimator by which to evaluate future MICOM electronics technology and packaging requirements.

A description of programs required to achieve the required technology in microelectronics is described. In addition, a criterion is presented which is used to determine which manufacturing technology program will produce the best return for missile microelectronics.

II. HYBRID THICK-FILM MICROELECTRONICS

Hybrid thick-film integrated circuit technology offers a number of advantages over other approaches. First, it requires less capital investment to establish fabrication facilities. There is roughly an order of magnitude difference in the cost of completely setting up a thick-film hybrid integrated circuit laboratory, and that required to build a complete monolithic integrated circuit fabrication laboratory. In addition, the cost per circuit produced is lower for a hybrid integrated circuit than for a monolithic chip in small volume production, e.g. less than 10,000 units. Monolithic integrated circuit chip costs can be driven will below thick-film hybrid circuit costs only by the influence of high volume production realized by simultaneoulsy fabricating many circuits on the same silicon wafer. In contrast, thick film hybrid circuits are usually fabricated manually one at a time or a few at a time on a ceramic type substrate. These economic considerations make hybrid thick-film technology an ideal starting point for microelectronic prototype development.

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Thick-film hybrid microcircuits offer some performance advantages but have certain attendant disadvantages. Thick-film patterns are screened on the substrate and subsequently fired at near 1000°C. The screening process produces inherently larger line widths than the photo lithographic process which is used for pattern definition in monolithics and sometimes in thin films. The minimum geometries with good thick-film technology are 4-mil lines and 4-mil spaces. For monolithics the state-of-the-art is approximately 0.2 mil for lines and spaces.

After fabrication, resistors which have been made by the process described previously can be actively trimmed using an air abrasive or laser trimming technique to produce resistor values within 1% tolerance. This figure compares with the typical ±20% tolerance of diffused resistors on a silicon chip. Thick-film resistors are limited in frequency response, however, and begin to appear partially reactive as the frequency approaches the VHF range. It is interesting that monolithic diffused resistors are also limited in frequency response because of their parasitic capacitance; therefore, it appears that thin-film technology offers the best approach for high frequency work.

In thick-film technology discrete capacitor chips are bonded onto insulating substrates to form capacitor elements because thick-film technology currently offers no practical way to fabricate capacitors. By employing separate capacitor chips for each individual capacitor, there is a wide range of capacitor values available for selecting the ones which lend some flexibility to the design. However, this process increases the cost of fabrication because each capacitor chip must be purchased and then manually attached to the hybrid microcircuit.

Thick-film resistors generally exhibit excessive electrical noise compared to other technologies. This becomes an obvious disadvantage when very sensitive high gain systems must be integrated. In these cases, thin-film resistors on a chip must often be attached to the thick-film substrate to improve the noise characteristics. Recent improvements in packaging techniques should lead to improved reliability and ease of assembly in thick-film hybrid circuits. For example, the leadless-inverted-device (LID), which evolved from the ceramic-channel carrier, provides a number of interesting features. The user never has to handle the chip itself or make the delicate wire bonds. The package provides protection for the chip from mechanical stress and shock during shipping and assembly.

Thick-film microelectronic technology has been well established as a viable microcircuit fabrication technique. In summary, its principal disadvantages are as follows:

a) No capacitors except those which are discretely bonded to the substrate.

b) No active devices.

c) High noise.

d) Large dimensions.

e) Relatively high cost of producing a circuit.

The advantages of this technology over monolithic silicon integrated circuits include higher voltage capability, better temperature coefficients, and closer tolerance of passive components.

Thick-film microelectronic components are limited in size reduction by the limitations of the silk-screen printing process. Hybrid technology alone cannot produce high density microcircuits; this disagrees with one of the strong trends in the industry. Further minimization as well as other capabilities can be obtained with another film process, i.e. that of thin films.

III. THIN-FILM MICROELECTRONICS

Thin-film microcircuits are fabricated from films of conductive, insulating, and resistive materials deposited on insulating substrates. In this technology, however, the films are much thinner, typically 50 to 50,000 Å, and have substantially different properties. The most common method for depositing a thin-film material on a substrate is that of vacuum evaporation. In this technique, the desired material is heated either by joule heating or electron bombardment in a vacuum chamber to its vaporization temperature. The evaporated gaseous material condenses on the nearby substrate and builds up a film of the material. Sputtering is another method of thin-film deposition which has become increasingly valuable because of its ability to produce films of materials which have extremely high vaporization temperatures. In sputtering, the desired material is bombarded with ions and the resulting collisions free atoms which deposit on the substrate. Thus, the process does not depend on extreme temperatures. Sputtering has been particularly useful in fabricating stable thin-film dielectric layers, such as SiO_2.

Thin-film technology can produce resistors and small value capacitors. Active monolithic integrated circuit chips can be bonded on the substrate to form a thin-film hybrid circuit. There is another possibility also. In recent years, interest has been growing in thin-film field effect transistor (FET) transistors--active devices which are fabricated by the same film process. Although these devices are still in developing stages, there has been a significant effort by RCA and more recently by Westinghouse in this area. At the 1975 International Electron Devices Meeting in Washington, D. C., Westinghouse presented a solid state display panel in which the image elements were driven by thin-film transistors in a large array.

Thin-film passive devices offer higher frequency operation; for example, microwave microelectronic strip-lines are generally made by this process. Better control of the component values and parameters can be achieved as well as the monitoring of critical parameters during fabrication, thus enhancing the reliability of the final product. Thin-film resistors are among the lowest noise components available. The thin-film process lends itself to being automated more readily than other approaches; in addition, this technology offers the possibility of producing active devices. The minimum size of thin-film components or minimum line width is limited by the resolution of the masking and photo-etching process similar to that used for defining patterns on monolithic chips. Thus the potential packing density is perhaps as much as an order of magnitude better with thin films than it is with thick-film technology.

For a laboratory with an advance thick-film fabrication process, the next logical step would be to initiate a complementary capability in the thin-film technology. The thin-film process will probably never replace the thick-film approach; however, it will provide additional capability an advantages in many applications as just described. It would serve as a step toward higher packing densities and smaller line widths and is the next sequential step toward monolithics. Therefore, it is recommended that the MICOM Microelectronics Laboratory expand its capabilities into thin-film fabrication as soon as possible.

IV. SILICON INTEGRATED CIRCUITS

The technique of fabricating complete microelectronic circuits in a wafer of single, crystal, silicon has allowed great advances in circuit packing density, and has brought about the age of large scale integration (LSI)--a level of integration corresponding to hundreds of equivalent gates per microcircuit chip. At the present time, only monolithic silicon technology is capable of producing cost effective, high density, microelectronic circuits and is making possible such innovations as the one-chip microprocessor. Monolithic silicon technology can be roughly divided into two groups: the MOS technologies and the bipolar technologies.

A. MOS Technology

MOS integrated circuits are almost exclusively digital. This fact is due primarily to the low transconductance of FETs over their bipolar counterparts--adequate for switching purposes, but not as attractive for linear signal amplification.

The p-MOS digital integrated circuit technology utilizes a p-channel MOS field effect transistor in the basic inverter gate with a load which is merely another MOS FET device biased so that it appears resistive. Diffused silicon resistors, quite common in integrated bipolar structures,

are rarely used in MOS circuitry because of the increased processing complexity they introduce. P-MOS integrated circuit technology was introduced first, but has faded in popularity in favor of n-channel MOS.

With a similar structure to that of p-MOS, but rather using n-channel FETs, the speed of propogation is increased; thus n-MOS continues to be a viable technology. Typical gate propagation delay times are in the 10 to 50 nsec range with a speed power produce of 10 pJ. A strong advantage for the MOS technologies is their fabrication simplicity because the basic n-MOS process requires only five photomasks and three diffusions or implants. A disadvantage of MOS devices is that device parameters depend on surface characteristics, which are more difficult to control than bulk material characteristics. In addition, the MOS devices are sensitive to static discharge, which can cause catastrophic circuit failure. For these reasons, the MOS circuits generally show lower reliability than those of the bipolar technologies.

A more recent MOS technology which is gaining popularity is the Complementary MOS (CMOS) in which both an n-channel and a p-channel device are used in a complementary arrangement. CMOS is easy to fabricate and yields gate delays in the 50-nsec range. However, a major difference in CMOS is that it draws no current except when changing logic states. Thus, at slow speeds it uses extremely little power. CMOS interfaces directly with n-MOS, has extremely high noise immunity, which is of significant concern in some MICOM applications, and operates over a wide power supply voltage range. CMOS does not have the packing density of n-MOS for LSI applications.

The relatively slow speeds of the standard MOS technologies can be overcome with the silicon-on sapphire (SOS) approach. In SOS, MOS devices are situated on silicon islands which sit on an insulating sapphire substrate. The dielectric isolation eliminates the parasitic capacitance associated with junction isolated devices and yields approximately an order of magnitude improvement in speed. THE SOS-CMOS technology has been developed intensely by RCA and others in an effort to build demand and reduce costs. Despite predictions just a few years ago that SOS would soon be cost competitive with silicon, it hasn't happened primarily because of the cost of using the sapphire substrate. Nevertheless, for military applications SOS offers increased speed, radiation resistance because of the dielectric isolation, and power speed products below 0.5 pJ. The disadvantages are cost and the material problems associated with making a low-defect density silicon epitaxial film. There is currently considerable debate within the industry as to the future of SOS, especially with strong competition from the new bipolar technologies such as Integrated Injection Logic (I^2L).

A new type MOS device has recently been devised, the so-called charge-couple-device (CCD). These are merely linear arrays of MOS devices in which charge packets can be clocked along a chain, shift register

fashion. If the charge packets represent binary data i.e. 0's and 1's, then the CCD serves as a serial dynamic memory circuit. Because each memory cell is reduced to a single MOS device in a chain, extremely high packing densities and therefore very large semiconductor memories on a chip are possible. Projected CCD memory costs are well below the other technologies reaching 0.05 cents/bit in 1978. Currently a 16K bit CCD memory chip is commercially available; this technology will certainly lead the way for high density silicon semiconductor memories.

An additional advantage of CCDs is that the charge packets can be used to represent sample points of an analog signal, because the amount of charge stored in each packet is a continously variable quantity. Thus an analog signal can be sampled, clocked through the CCD at the desired rate, and appear reconstructed at the output, but delayed in time. Thus the CCD can function as a solid state delay line and prove very useful in signal processing and correlation applications.

B. Bipolar Technology

The second major group of silicon microcircuits are the bipolar technologies, both linear and digital. Considering the digital area first, the technology of greatest popularity for both small scale intergration (SSI) and medium scale integration (MSI) is the transistor-transistor-logic (TTL) family. These devices, which are fabricated from standard bipolar processes, are reasonably fast but require a moderate amount of power. This technology is improved by the addition of Schottky clamps which prevent the active devices from saturating, and thus decrease the delay times. A further refinement, the so-called low power Schottky TTL is gaining strength in the industry and is somewhat competitive with other technologies in LSI applications, particularly where higher speeds are required. It lacks packing density, but is only a factor of two worse than CMOS, and has gate delays in the 1-to 10-nsec range.

Until 1972, the MOS technologies were moving towards domination of the LSI market. In that year, I^2L was invented; this fresh bipolar approach gave new life to bipolar LSI. I^2L is very dense, a factor of three better than CMOS, and can be made as fast as 10 nsec per gate delay, or operated at slower speeds and lower power making it very flexible. For this reason, I^2L is now being used in applications ranging from very low power digital watch chips to moderately fast microprocessor chips. The speed power product of I^2L is in the 0.5-pJ range which is very attractive. Schottky I^2L where Schottky diodes are placed in a series with each of the outputs to limit the signal excursion has brought this number even lower.

I^2L is very easy to process with standard bipolar monolithic processes, and can be made with only four photomasks and two diffusions

or implants. I^2L is an extremely valuable technology in that it offers a bipolar technique with its associated higher reliability, which is completely compatible with LSI. I^2L will undoubtedly make progress as a random logic technology and in the memory area as well, because of its high packing density. In fact, a 4K I^2L random access memory (RAM) is soon to be announced by a commercial manufacturer.

Emitter coupled logic (ECL) is designed for very high speed applications where power can be sacrificed to achieve speed. It will probably never be viable as an LSI technology because of its poor packing density, and large power delay product.

Linear signal processing devices, such as op-amps, multipliers, phase locked loops, etc., are almost universally made by the monolithic silicon bipolar technology. The sizes of components used in these microcircuits are generally larger than those used in digital circuits because of a higher break-down voltage requirement.

The development of I^2L should impact the linear integrated circuit world because of the interesting fact that I^2L is completely compatible with bipolar linear processing. In other words, digital signal processing via I^2L technology can be put on a linear integrated circuit chip with no additional processing steps. Looking ahead, it might be expected that there would soon be developed many kinds of linear/digital circuits on a chip, such as A/D converters, digital filters, etc.

V. INTEGRATED OPTICS

Integrated optics defines the discipline in which an attempt is made to apply thin-film technology to optical circuits and devices to obtain better and more economical optical systems through the application of integrated circuit techniques. If these modern optical transmission systems are to be viable, they must be as economical, rugged, and small as comparable systems employing beam-mode propogation via lenses and mirrors.

The development of a thin-film laboratory places MICOM in a position to develop an integrated optics capability easily. However, this field is relatively new and much of the work carried out at the present time is highly experimental. Because other priorities at MICOM, such as the development of thin-film and monolithics facilities, are more important to the enhancement and usefulness of the laboratory, it is recommended that the area of integrated optics not be attacked until a later date.

VI. COMPUTER-AIDED DESIGN

Computer-aided design (CAD) has had a profound influence on microcircuit design and layout. There are basically two functions which CAD plays in aiding the designer. First, computer circuit simulators ease the work of the engineer in designing a circuit configuration. The computer can provide the designer with almost instantaneous feedback on the circuit which has been devised. For integrated circuit development the circuit simulator, Simulation Program with Integrated Circuit Emphasis (SPICE), has emerged as a popular and extremely valuable aid. The program is currently being used at Bell Labs, Texas Instruments, and elsewhere for verification of circuit performance before integrated circuit designs are committed to fabrication. SPICE provides all three modes of analysis: ac, dc and transient. A more sophisticated program with full Monte-Carlo capability is the program, ASTAP, developed by IBM. This program has great capability, but the extremely large computer memory required and the long run-time of programs make it extremely expensive to use. It is often not the best use of resources. For an up-to-date look at the many CAD and analysis programs the reader is referred to the recent paper by Blattner*.

The second area where the computer has made significant impact on integrated circuit design is in the interactive graphics approach to lay-out. With the computer taking much of the repetitive labor and manual drafting out of producing a phototool for integrated circuit fabrication, the designer can produce better quality work in shorter periods of time.

The MICOM Prototype Hybrid Laboratory has a Gerber digitizer and pattern generating system. This state-of-the-art facility can be used for producing phototools for future fabrication of thin-film microcircuits and/or monolithic integrated circuits.

VII. RECOMMENDATIONS

This report has suggested that the MICOM Prototype Hybrid Micro-electronic Laboratory, which is presently tooled for thick-film micro-circuit fabrication, should expand to include thin-film and monolithics as soon as it is practically feasible. Much of the justification for

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*Blattner, D. J., "Choosing the Right Programs for Computer-Aided-Design," Electronics, April 29, 1976, pp. 102-105.

this statement has been previously discussed. In addition, it should be noted that although reliability is important to commercial semiconductor manufacturers, factors such as radiation hardening, extreme temperatures, and the like are of little interest to these companies because their production facilities are kept busy simply supplying the commercial market. These companies are very secretive and protective of their manufacturing processes. Thus, failure to set up MICOM facilities which keep pace with state-of-the-art processing techniques is tantamount to being totally dependent upon outside contractors and their processes. Because of the extreme importance of MICOM's mission and the fact that MICOM has specific interests and requirements, it would appear to be only prudent to maintain an in-house research and development facility with complete process control for the development of custom integrated circuit chips.

Future missile systems will require integrated electronic systems with complexity and size constraints which demand monolithic LSI chips. It is recommended that serious consideration be given to developing I^2L capability as soon as possible. As stated earlier, missile systems contain both analog and digital systems; therefore, a bipolar processing line capable of developing high density digital and linear circuits would be advantageous.

A. Projects

The appendix of this report contains a list of projects which should be undertaken by MICOM. The projects cover a wide spectrum of technologies; yet the focal point for all the projects is the development of microelectronics which has attendant adjectives such as economical, failure resistant, maintainable, reliable, and testable. The projects are subdivided and categorized for convenience into the following areas:

a) Materials and components

b) Design techniques in digital systems

c) Computer aided design

d) Processing techniques

e) Testing and reliability

f) Technology

g) Applications

h) Packaging

Each project listed in the following section is placed within the area with which it is most concerned even though it must be recognized that some of the projects may appear to be applicable to more than one area because of the inherent interconnections which exist among the areas.

The projects proposed in this section will have the following format:

Priority	Research Areas	Justification	Manufacturing Methods and Technology (MM&T) Task

Priority 1 is used for the highest priority items; items with priority 3 are those with lowest priority. The research areas represent specific topics of investigation which should precede the MM&T task listed in the fourth column and justified in the third column.

VIII. SELECTION AND CRITERIA FOR MM&T PROGRAM

B. Problems and Programs

A problem exists when there is dissatisfaction with things as they are. By its existence, a problem stimulates a desire to change or correct something, to bring something new into being, or to reduce if not eliminate the dissatisfaction. The disappearance of the dissatisfaction signifies that a solution of the problem is in hand.

A program brings the problem and its solution together. Indeed, by its very existence, the program offers hope that a particular dissatisfaction will vanish after the program is successfully excuted.

C. The Ratio of Cost to Return (C/R) as a Criteron for Economic Analysis

The cost of a program measured against projected savings, expressed in dollars, clearly relates two factors of primary significance. These two, formed into a C/R ratio, result in a criterion for economic analysis. It is a number which is hopefully equal to unity or less; however, a serious question arises as to whether or not the "correct" value of this ratio should be set a priori and then used by itself to evaluate a proposed program.

The C/R ratio can become a comprehensive criterion if the two terms involved are properly defined. The numerator, or cost of the program, can be and is now understood to mean the sum (in dollars) of the contract amount and the monitoring costs including government overhead, government personnel involved, and government furnished equipment (GFE). The denominator, the return to the government from the program, has a greater potential for flexibility than the numerator. To give it a comprehensive definition would be sufficient to make the C/R ratio an adequate measure to use in rank-ordering MM&T projects. To do so, however, would mask, or perhaps obliterate as a separate and distinct entity, the direct savings anticipated in manufacturing and production costs. Such savings are significant in themselves and perhaps should survive as an identifiable factor in project evaluaton.

If the denominator of the C/R ratio is restricted to mean the direct savings (in dollars) to be realized in manufacturing and production costs, the ratio itself can become the first consideration in economic analysis.

This leaves unresolved the question of what the numerical value of the ratio should be for a project to be deemed worthy of support.

The need for a rational alternative to the arbitrary designation of a numerical value for the C/R ratio is based on the premise that a project may be in the national interest and/or may have military value even when the C/R ratio is unfavorable. Moreover, the introduction of other considerations in the evaluation process may avoid the pitfall of denying a project of intrinsic worth only because its C/R ratio fails an arbitrary standard. Likewise, the acceptance of a project without lasting value may be avoided. In addition, the inclusion of other considerations may provide a more meaningful guide for the persons of experience who must finally exercise the judgment and make the decision on which projects are worthy of support. Justification for a decision can be provided by a figure of merit which involves, in a known and rational manner, significant considerations in project selection in addition to cost and return.

D. Development of Additional Selection Criteria

A subjective/quantitative method involving a question format was developed as a trial approach. Its status is given in Appendix A. A firm basis for a completely objective approach is unlikely to be found. Whatever method finally evolves will undoubtedly require substantial subjective input, even though it may be more quantitative than the present trial approach.

Considerations in project selection are implicitly involved in the questions (Appendix B). The questions may prove to be a check list which can become a basis for the development of more quantitative criteria. They are written in a direct style so that they can be answered "yes" or "no," with a "yes" answer having a favorable impact on the project value.

A serious attempt was made to eliminate redundancy in the questions. True independence is probably not possible because all the questions are intended to be related to the primary matters of cost benefits and project value. Whenever possible, cases were avoided where the answer to one question suggests or implies the answer to another or where one answer makes other answers irrelevant. Some use of the method will be required and some study of the questions by others will be necessary to determine the extent to which these goals are realized.

The matter of timeliness is considered in the questions only from the standpoint of "can the project bo finished on time" and "can it be

finished in time to have an impact on current production and/or on production already under procurement." Timeliness with regard to Research and Development scheduling and to the scheduling of future procurement was not included explicitly, although these are recognized as significant factors in the scheduling of future fund allocations and procurement of MM&T projects. Moreover, it is recognized that the project value determined by a method similar to the trial approach suggested here may vary up or down from fiscal year to fiscal year, depending on Research and Development, procurement scheduling, and military priorities.

E. Future Development of Selection Criteria

The trial method presented in Appendices A and B identifies many of the significant factors in project evaluation. The figure of merit calculated by the method is a number related to a project by means of a small amount of arithmetic based on human choices of answers to questions which were written and weighted by humans.

It is a beginning, nonetheless, because it contains information which can be used at the start of a step-by-step development of a symbolic evaluation model.

The questions in Appendix B can be screened for two lists of variables. The first list, those variables under the control of MM&T, and the second, those variables not under the control of MM&T, can be studied to find functional relationships. The next task would be to express the relationships in mathematical form. When this is accomplished to the extent possible, the process of optimizing the effect of the control variables can begin.

This approach obviously is much easier to outline than to carry out. Much feedback from MM&T personnel will be needed. The central objective of developing a rational means to rank order a given list of projects in any of five future fiscal years is formidable but not without hope of attainment at least to some degree. Any small advance may have value in itself, in addition to being a starting point for the next step.

Appendix A. STATUS OF A SUBJECTIVE/QUANTITATIVE TRIAL APPROACH TO THE DEVELOPMENT OF CRITERIA FOR PROJECT SELECTION (THE F METHOD)

1. Evaluating F, a Figure of Merit

The answer to each question in Appendix B is to be one of the following six:

Answer	Weight of the Answer A_1
Strong Yes	A_6
Moderate Yes	A_5
Weak Yes	A_4
Weak No	A_3
Moderate No	A_2
Strong No	A_1

where $A_6 = 100 > A_5 > A_4 > \ldots A_c > 0$ and the A_1 are integers.

To find a weighted average of the answers to the questions in a given category, the following procedure is used:

Let Q_{ij} by the weight of question i in category j and A_{ij} be the weight of the answer to question i in category j. Then, $\overline{A_j}$, the average of the weight of the answers A_{ij}, in a given category j weighted with respect to Q_{ij}, is given by

$$\overline{A_j} = \frac{\sum_{i=i}^{i=m_j} A_{ij} Q_{ij}}{\sum_{i=1}^{i=m_j} Q_{ij}} \qquad (1)$$

where m_j is the number of questions in category j. Finally, $\overline{A_p}$, the overall average weight of the answers for project p, weighted with respect to the category weights, is given by

$$\overline{A_p} = \frac{\sum_{j=i}^{j=c} \overline{A_j}\, G_j}{\sum_{j=1}^{j=c} G_j} \qquad (2)$$

where c is the number of categories and G_j is the weight of category j. An overall figure of merit, F, for a project may now be defined as

$$F_p = \overline{A_p} \left(\frac{R}{C}\right) p \qquad (3)$$

where $\left(\frac{R}{C}\right) p$ is the inverse of the cost to return ratio for project p, previously evaluated.

It is worth saying that F_p is only a number related to a project by means of a small amount of arithmetic based on human choices of answers to questions which were written and weighted by humans. However, the F_p are numbers and as such can be listed from lowest to highest, thereby giving a rank order to the project represented by each F. The highest F represents the most favorable project; the lowest F, the least favorable.

It is clear that the project evaluator has an alternative. He may use $\overline{A_p}$ from Equation (2) and the C/R ratio as two separate numbers rather than combining them into F as proposed in Equation (3).

2. Source of Weighting Factors A_{ij}, Q_{ij}, and G_j

It is proposed that these factors be weighted on a scale 1 to 100, with 100 being the most favorable and 1 the least favorable. The weights of each factor should be obtained by a consensus of experienced persons from contractors and government. The weights finally assigned should be determined by the government and not necessarily be made available to prospective contractors. Dissemination of the weights to contractors may prove to be beneficial because it would encourage the development of projects with high overall value.

3. Source of Answers to the Questions

There is a choice to be made among six possible answers to each question, as previously indicated. The choices are to be made after study of the project proposal and after a decision has been made that the project is worthy of evaluation. The choice of answers can be made while the C/R ratio is being determined.

Ideally, the choice of answers should be made by persons other than those involved in the determining of the weighting factors. It is

unlikely that this will be possible, so the choices will probably have to be made by a project evaluator. If more than one evaluator is used for a given project, the differences in their choices of answers can be reconciled at the beginning, before F is determined, or at the end by reconciling the differences in the F's they obtain.

4. Objectivity

It is obvious that complete objectivity should be sought by persons involved in determining the weighting factors and in making the choices of answers.

5. Consistency Check

The persons involved in determining the weighting factors should at the same time be asked to rank a group of perhaps 10 Hilton Head projects. The consenus of their overall rankings should then be set aside to be checked against the ranking determined by the ordering of the F's obtained in the procedure outlined here.

A good agreement will indicate that the weighting factors are substantially current. A poor agreement will indicate some fault in the F method which needs correcting.

A revision of the weighting factors may be in order. If this should bring about agreement, then there again is a good basis for further use of the F method.

If revision of the weighting factors cannot bring about acceptable agreement, then it will be necessary to restudy the questions and their answers to see if the F method can be made into a reliable and consistent guide for evaluation by revision of the questions, answers, and categories.

6. Extension of the F Method to Include Consideration of the Different Systems and Subsystems Involved in Project Proposals

The projects proposed at Hilton Head normally related to a subsystem of a missile system. Two multiplying factors can be applied to F to take into account the relative importance of the subsystem.

The first factor is the weight assigned to the subsystem in relation to the missile system of which it is a part. It is suggested that this factor be determined at a level no lower than US Missile Research and Development Command (MIRADCOM).

The second factor, which ranks the importance of the missile system in relation to other missile systems, probably must be determined at higher levels. It is of the nature of a command decision.

Trial and application of the F method need not wait for the determination of these two additional weighting factors. As a first approximation, equal weight can be assigned to all subsystems; equal weight can be given to all systems. In such a case, F will then stand alone as the figure of merit to be applied with judgment by persons of experience in ranking the projects.

Similarly, when F is used alone as a figure of merit, it must not be forgotten that there is an implicit assumption that all missile systems and subsystems are considered to be of equal importance.

Appendix B. QUESTIONS TO BE ANSWERED TO EACH PROJECT OUTLINED IN THE PROCEDURE OF Appendix A.

Category A. Cost, Regulatory, and Conservation Considerations

1. Is a cost-driving practice* eliminated, replaced, or simplified at reduced cost?

2. Is a bottle-neck practice replaced with one less critical?

3. Does the alternative practice reduce assembly costs?

4. Is the alternative practice compatible with the production line?

5. Does the alternative practice require the relaxation of specification and design requirements**?

6. Can the alternative practice be adapted to improve the producibility of other systems, subsystems, components, or parts?

7. Will costs of inspection and testing be reduced?

8. Will consumption of strategic and/or cost driving, high performance materials be reduced**?

9. Will consumption of energy be reduced by the alternative practice?

10. Is there a favorable impact on EPA and OSHA requirements?

Category B. Technology Transfer and Security Consideration

1. Will there be new technology which can be transferred?

2. Can costs be reduced elsewhere† by introduction of the new technology?

3. Will there be savings in energy or materials which can be transferred?

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*"Practice," as used in any of these questions, refers to any manufacturing method or process.

**If ther answer is "yes" (in any degree), the tradeoffs with mission will be evaluated by MIRADCOM. Any contractor answering these questions is invited to attach his input on this point, so that it may be included in the MIRADCOM evaluation.

† Government owned, government operated (GOGO); government owned, contractor operated (GOCO); or prime or subcontractor.

4. Can environmental improvements or safety benefits be transferred?

5. Is the new technology such that security measures should be introduced to classify all or part of it?

Category C. Considerations Involving a Return to the Government

1. May a return be expected from patentable features of the new technology?

2. May a return be expected from transfer of the new technology to the private sector?

3. Will the government benefit by making the new technology available to the private sector without seeking a patent?

4. Is the new technology such that a return may be expected from reduced life cycle costs of the system?

5. May a return be expected if the new technology is transferred to GOCO or GOGO operations elsewhere or if the contractor transfers the new technology within his own GOCO or private operations?

Category D. Timeliness and Location Considerations

1. Is the development of the new technology compatible with Research and Development and Procurement scheduling?

2. Can the project be completed without a cost over-run?

3. Can the proposed time schedule be met?

4. Will there be greater cost with the same or less return if others do the project or if it is done in-house?

5. Will the project be completed in time to have an impact on manufacture of production equipment or tooling?

6. Will the new technology be available when it can have the greatest impact on costs?

7. Will the project measure feasibility of production equipment or tooling in time to impact current or future production of the product?

8. Will the project be completed in time to impact on manufacturing processes related to the product?

9. Will the project be completed at a time when it can favorably influence the cost of future production?

10. Will the project be completed at a time when it can favorably influence the cost of current production?

Appendix C. DESIGN AND MANUFACTURING: A RECOMMENDATION FOR ENHANCED COOPERATION

The MM&T Directorate ideally becomes involved with a system or one of its elements after it is designed. This procedural requirement is interpreted to mean that while MM&T is not responsible for the design function, it must be concerned that the design is not itself a major cost driver and does not have an adverse effect on producibility. MM&T should work with designs which give adequate consideration to maintainability, transportability, durability, usability, and other life cycle cost factors. Designs not adequate in these respects would scarcely seem to qualify for economic analysis of their producibility.

The interrelationship between design and manufacturing cost was often mentioned in the papers presented at the AMC-sponsored Missile Manufacturing Technology Conference at Hilton Head Island in September 1975. It is thought-provoking to ponder the question of what savings in the cost of a missile can be realized by a closer relationship between these functions at contractor level.

To address this question, it is recommended that a second Missile Manufacturing Technology Conference be called on the subject of "Unification of Missile Design and Manufacturing Technolgoy." The aim of the second conference will be to concentrate on specification and design standards as cost drivers and what to do about them.

Such a conference can invite papers from contractor-manufactures (both primes and subs) written jointly by a designer and a manufacturing engineer (or one performing that function). Each paper should include a rationalization of past differences between the two viewpoints and a recommendation of what may be done in the future to resolve them in the interest of cost savings.

The conference will be a low cost effort with a possible high return. Bringing together the different sets of people involved in design and in manufacturing may produce interesting and beneficial results in contractor organization and in future cooperation between these two now largely separate elements. Moreover, the conference should be a source of ideas as to how enhanced cooperation between design and manufacturing will work and how it will bring about savings in missile costs.

MATERIALS AND COMPONENTS

MM&T

Priority	Research Area	Justification	Task
2	To determine the speed, reliability, etc., of acoustic wave devices and the manner in which they can be efficiently applied in microelectronics missile technology for a) Analog Signal Delays b) Real Time Correlation Techniques c) Advanced Signal Processing Techniques such as Image Enhancement	Future missile systems will require for guidance, control, and signal processing, time delays, correlation capabilities, that can be efficiently integrated with other active circuitry.	To develop manufacturing processing techniques for acoustic wave devices which are capable of satisfying these requirements in a reliable and compact fashion.
1	Deployable missile systems should have attendant energy storage devices which have long life, are light, and are powerful. A research program should be initiated to specify the types of devices which are viable in this situation and determine the cost/performance factors which affect development.	As the electronic capability of missile systems increases, the need for compact, reliable power sources will increase.	To develop manufacturing processes for producing high reliability, high density energy storage devices.
3	To develop techniques for examining high strength adhesion of thin-film and thick-film substrates. The physisorption and chemisorption mechanisms should be examined in particular.	Substrates for electronics used in the hazardous environment of future missile systems will need increased strength to withstand vibration and stress.	To develop production techniques for manufacturing new high strength adhesion techniques for use with substrates.

DESIGN TECHNIQUES IN DIGITAL SYSTEMS

MM&T

Priority	Research Area	Justification	Task
1	To develop techniques to implement multilevel logic into existing systems to improve the density of information contained in a single memory cell.	Advanced missile systems will require the most sophisticated electronics available to reduce size and power and increase density.	To develop production techniques to implement multilevel logic into existing missile systems.

CAD

MM&T

Priority	Research Area	Justification	Task
1	To investigate the development of an economic raster scan color graphics system employing microprocessors which have rotational and translational capabilities and employ different colors for different levels of masking.	Color graphic systems necessary for CAD are very expensive and not cost effective.	To develop manufacturing techniques which employ low cost color graphics for microcircuit design.
2	To investigate the development of graphic input devices for inputting microcircuit designs into the production process.	Graphic input devices would increase the speed and efficiency of the microcircuit production process.	To integrate graphic input devices into the microcircuit manufacturing line.
2	To investigate the development of a minicomputer network for the layout and analysis of integrated circuits.	A minicomputer network for CAD of integrated circuits would appear to be more cost effective than the current use of large computers.	To replace the large computers used for circuit analysis in the manufacturing process with a minicomputer network.

PROCESSING TECHNIQUES

MM&T

Priority	Research Area	Justification	Task
2	To evaluate the minimum line widths which can be obtained with the E-Beam lithographic process including the effects of various E-Beam photo resists, beam energies, exposure times, etc.	Future missile systems will require very small line widths and extremely high packing density.	To develop production techniques using the E-Beam (submicron) lithographic process.
1	Advances in microelectronic processing technology are required for the development of higher speed logic gates. Research should be conducted to examine potential candidates, e.g., SOS or dielectrically isolated ECL.	The present speed limitations on logic gates are in the low nanosecond range.	To develop manufacturing capability for new technologies such as SOS for subnanosecond logic gate systems.
2	To analyze techniques for achieving multilayer metallization systems including an evaluation of minimum line widths for each level, interlevel short density, dielectric characteristics, and reliable vias.	High density in bipolar integrated circuits requires multilayer metal-film interconnections which significantly complicate the processing sequence.	To develop manufacturing processes for simple multilayer metallization systems on monolithic integrated circuits.
1	To develop and evaluate isolation techniques for high density LSI integrated circuits (IC) using dielectric isolation.	The capability of reducing isolation areas in IC elements, thereby making chips denser, cheaper, and faster will be more important in future missile systems.	To develop production techniques for anodizing silicon; an economical way to isolate IC elements and applicable to MOS or bipolar technologies.

PROCESSING TECHNIQUES (Continued)

MM&T

Priority	Research Area	Justification	Task
3	Research should be performed which explores the fabrication and efficient use of charge transfer devices (CTD) for processing analog signals in such a way as to obtain the timing and control properties inherent with digital signal processing.	Signal processing in radar and electronic countermeasures (ECM) systems can be enhanced with the use of serial transfer structures.	To develop manufacturing processing techniques for the production of CTD.
3	Screened or batch-processed resistors are currently not compatible with the co-fired tape process of hybrid technology. Research should be performed to determine methods for eliminating the need for chip resistors thus enhancing the cost/performance characteristics of this process.	The co-fired process is a viable technique for hybrid technology because it offers the advantages such as multilayer, double-sided assembly for high density, superior film adhesion, and eliminates the need for a high cost metal package.	To develop production techniques for the co-fired tape process to take advantage of its inherent capabilities.
3	Thin-film resistors have better noise qualities and temperature and voltage coefficients than thick-film resistors, but the upper range of resistors is limited to approximately 200 kΩ compared with 200 MΩ for thick-film resistors. Methods for extending the upper range of resistive systems in thin-film processes should be determined.	The limited range of resistivity obtainable on a single substrate in multilayer thin-films can be broadened by integrating thick-film resistors and traditional thin-film resistors on the same substrate.	To develop manufacturing techniques for producing a multiple resistivity thin-film/thick-film process.

PROCESSING TECHNIQUES (Continued)

MM&T

Priority	Research Area	Justification	Task
2	Complicated fabrication and assembly processes of the future will require advanced programmable automatic systems with capabilities far beyond those currently available to reduce labor costs and improve processing speed. The use of industrial robots for complicated assembly of future electronic systems should be evaluated. The use of these devices in each of the following areas should be examined: a) Printed Circuit Boards b) Thick-Films c) Thin-Films d) Monolithics	As tactical missiles become smaller and the microelectronics for guidance and control becomes denser and more sophisticated, fully automated assembly, interconnection, and packaging of the missile electronic systems will be required.	To develop manufacturing techniques which employ automated transports, mechanical robots, optical aligners, etc., for fully automating the assembly, interconnection, and packaging operations in the production of electronics for guidance and control systems.
1	Research which explores the use of electro-optics, which is compatible with thin-film active device technology is required to obtain the considerable cost savings and reliability which could be achieved by placing the display and sensor elements on the same substrate with the control and processing circuitry.	Display panels and sensors for use in missile systems will require high reliability and extremely low power consumption for portable operation.	To develop manufacturing techniques for producing thin-film electro-optic displays and sensors.

PROCESSING TECHNIQUES (CONTINUED)

MM&T

Priority	Research Area	Justification	Task
1	To investigate the possible techniques for fabricating energy sources directly into integrated circuits to provide total nonvolatile systems which are self-powered.	Complex missile systems often require nonvolatile electronics. Long term storage in the field can lead to failure of conventional forms of power.	To develop production techniques to fabricate LSI integrated electronics with new power sources integrated into each LSI system.
1	To perform an investigation of merged device structures to increase packing density for more efficient use of silicon with both bipolar and MOS devices.	Future missile system electronics will require increased packing density.	To develop manufacturing technique for the production of merged device structures.
1	To perform an investigation of carrier domain devices for increasing the signal processing capability of an integrated circuit.	Future guidance and control systems must take advantage of increased packing density to be economical.	To develop manufacturing processes for the production of carrier domain devices.
1	The three primary limitations of MOS speed capability are due to device transconductance, stray capacitance, and the voltage swings required to change state. A research program should be developed to attack these speed limiting problems in order to make these devices more applicable to microelectronic-based missile systems.	Missile systems of the future will require increased speed to handle the expected higher data rates.	To develop manufacturing techniques for processing improved MOS devices which minimize the speed limiting characteristics of current units.

PROCESSING TECHNIQUES (CONTINUED)

MM&T

Priority	Research Area	Justification	Task
1	To investigate LSI CMOS technology to develop techniques for fabricating high density CMOS logic applicable to LSI circuits. An existing limitation of the application of CMOS is its low packing density. The possibility of using merged structures to improve CMOS packing density should be investigated.	Certain logic functions can often be simply realized with CMOS; the MOS technology also provides a large noise margin and CMOS provides high density without the added process complexity of multilayer metallization.	To develop CMOS production processing capability for implementing standard logic functions in silicon gate MOS technology.
1	To investigate the fundamental limits on the size and packing density of MOS integrated curcuits and seek new fabrication approaches to improve upon these limits (e.g. how can MOS devices be merged into the bulk silicon to take advantage of the space normally wasted in standard IC technologies).	Future missile electronics will require the placement of numerous devices in close proximity on an IC to obtain high packing density of active devices.	To develop the capability of manufacturing and improving high density MOS integrated circuits.
2	To investigate the fundamental performance and limitations of silicon MOS devices and seek new materials, structures, etc., which will extend present limits of performance.	New techniques are required to enhance the basic MOS performance.	To develop production techniques for high performance MOS technologies.

PROCESSING TECHNIQUES (CONCLUDED)

MM&T

Priority	Research Area	Junstification	Task
2	To investigate MOS devices fabricated on II-IV and III-V compound semiconductor substrates for improved performance.	New missile systems will require switching speeds for MOS which are faster than those currently obtainable.	To develop materials processing operations which achieve very high transconductance MOS devices applicable to LSI integrated circuits. VMOS and DMOS techniques may be applicable.

TESTING AND RELIABILITY

MM&T

Priority	Research Area	Justification	Task
3	Research should be performed which is aimed at the development of techniques for inherently designing into the electronics the capability for self-diagnosis and repair. Hardware redundancy may be required. The optimum manner in which to employ redundancy such as triple modular redundancy (TMR) and voter systems should be determined.	Some future missile systems will require extreme reliability.	To develop techniques for building into the electronics two important reliable features: 1) TMR which is capable of withstanding selective failures. 2) Self repair electronics capable of diagnosing and repairing failures.
2	A viable research program in the area of missile electronics would be to develop measurement techniques for predicting component and system reliability properties via the noise statistics of the devices.	Early estimation of system reliability would save time and cost.	To develop on-line processing techniques for determining component reliabiltiy via noise measurements.
3	To expedite testing and fault detection in LSI circuits, selection criteria for identifying and extracting test points to facilitate fault detection/isolation are required, i.e., how the circuits can be completely tested with the fewest test sequences and in the minimum amount of time.	Complicated LSI circuits are difficult to test. Early fault detection within the manufacturing line can reduce cost and save time.	To implement within the manufacturing process a procedure for supplying test points in LSI circuits which will facilitate fault detection.

TESTING AND RELIABILITY (CONTINUED)

MM&T

Priority	Research Area	Justification	Task
1	Manufacturing costs could be reduced and yield improved if the correlation between failure modes and process parameters could be identified. Research should be performed to determine the relationship between device failure modes and process parameters to optimize the manufacturing line for device failure reduction.	Correlation of process parameters and device failure modes can lead to improvements in production techniques.	Adjustments in manufacturing parameters and processes which have been correlated with device failure modes should be performed to minimize product failures.
2	To investigate techniques to detect reliability problems early in the manufacturing prccess. The fundamental parameters to detect, measure, sample, test, etc., should be identified.	IC testing is expensive and time consuming.	To develop real time techniques such as x-ray/TV or voltage contract/scanning electron beam microscope (SEM) systems for nondestructive analysis of devices during manufacture to improve yield and reliability.
2	To analyze optical scanning techniques including pattern recognition methods to determine the proper system configuration and algorithms to be employed for defect detection.	Defects such as pits and pores must be detected in order to improve the reliability of printed wiring boards (PWB)	To develop and automatic handling and inspection system employing an optical scanner for defect detection.

TESTING AND RELIABILITY (CONCLUDED)

MM&T

Priority	Research Area	Justification	Task
2	To develop techniques for sectioning LSI chips in order to correlate device structures with failure modes via a transmission electron microscope.	Failure analyses of LSI circuits with detailed device geometries and crystalline structures can most easily be accomplished through a cross-sectional analysis of the circuit.	Develop transmission electron microscopy system for LSI circuit analysis (cross-sectional) in a production environment.

TECHNOLOGY

MM&T

Priority	Research Area	Justification	Task
1	Fiber optics is a viable technology for use in missile electronics. Research areas of investigation of this technology include bandwidth, cross-talk, reliable coupling, electrical optical signal interface, amplification, stress analysis, mechanical stability, optimum design for analog or digital data, etc.	The performance and reliability of certain elements such as the missile wiring harness could be improved with fiber optics to limit electromagnetic pulse (EMP) and noise immunity.	To develop manufacturing, assembly, and testing techniques for fiber optics.
1	Smart tactical weapon systems of the future which are smaller and more lethal will employ microprocessors and require large memory capacity. The optimum advanced technology for use in high density memory devices which will produce cheap reliable and nonvolatile memories should be determined.	As the guidance, control, and data processing requirements of missile systems become more complex, the data storage requirements will become more stringent.	To develop production methods for implementing the memory technology identified in the previous research into the missile systems.

APPLICATIONS

MM&T

Priority	Research Area	Justification	Task
1	Future missile systems will employ many displays. The optimum display elements and their configuration should be determined from a cost/performance standpoint. Typical candidates are: Plasma Planar Liquid Crystal Magnetic Bubbles Thin-Film Electroluminescent	Typical display systems used in missile systems technology are very expensive, fragile, and consume much power and space.	To develop manufacturing capabilities for the economic production of small, highly reliable, rugged, and cost effective display elements, e.g., thin-film electroluminescent displays.
2	To evaluate the capabilities and process requirements for employing microelectronic elements as sensors and placing them within an IC chip, e.g., an electronic thermometer can be built using a diode or transistor as the sensor.	Future electronic systems in missiles will have speed requirements which dicate that certain sensors should be an integral part of the electronic data processing equipment.	To develop processing techniques for integrating sensors and other devices into the microcircuit chip, e.g., thin-film thermocouple.
1	Highly efficient infrared (IR) detectors with a good uniform response are needed for field sensors to detect objects of military importance. A research project should be performed which is aimed at determining methods for fabrication on a single chip large scale arrays of IR detectors for detecting long wavelength signals and the attendant LSI electronic signal processing circuitry.	Gun barrels, engines, and other items of military importance which require detection radiate power in the IR spectrum.	To develop manufacturing processes for producing small systems containing arrays of IR detectors with the attendant LSI data processing circuits for use as field sensors.

APPLICATIONS (CONTINUED)

MM&T

Priority	Research Area	Justification	Task
1	To examine logic techniques which are capable of reducing costs through higher reliability, fewer packages, and lower chip counts. Research aimed at evaluating the use of PLAs which are capable of eliminating the need for most random logic and are uniquely adaptable to any logic design problems should be initiated.	It would appear that within the near future programmed logic may be a useful and viable alternative to random logic.	To develop production techniques for manufacturing multifunction PLAs in a variety of architectures, sizes, and speeds.
2	LSI circuits used in guidance, control, and data processing systems will be required to withstand nuclear radiation. Examine I^2L, SOS, SO spinel, thin-film transistors and the failure mechanisms associated with them when exposed to nuclear radiation.	Missile electronics in order to be effective, must be capable of withstanding limited amounts of nuclear radiation.	To develop manufacturing techniques for the production of LSI circuits which are failure resistant to nuclear radiation.
2	To determine the optimum system configuration and the repertoire of testing algorithms to be used in a small, lightweight, and portable system for the automatic checkout of missile electronic systems.	In order to enhance maintainability and provide an operational status check of field-deployed missile systems, a system exerciser should be developed.	To design and construct an electronic exerciser for long term storage systems data useful for resistability, qualitative assurance (QA) analyses in the manufacturing line.

APPLICATIONS (CONCLUDED)

MM&T

Priority	Research Area	Justification	Task
1	To investigate the use of solid state optically coupled systems such as light emitting diode (LED)/ silicon transistor optical couplers/isolators in missile electronics, characterize present optical devices, and develop new ones to satisfy future needs.	Sophisticated missile electronics in order to be reliable must possess high noise immunity and isolation capabilities.	To develop processes for optical signal coupling in missile electronics.

PACKAGING

MM&T

Priority	Research Area	Justification	Task
3	An analysis of basic IC elements is required to determine the types of packaging materials and packaging configuration for maximum resistance to nuclear radiation.	New economical and efficient packaging techniques will be required for radiation survival.	To develop techniques for building circuits which can withstand radiation.
1	To evaluate thin-film material systems and flexible substrate materials for producing flexible thin-film microcircuits.	Future packaging constraints of missile systems will require microelectronic packaging innovations such as circuits of flexible substrates.	To develop automated production techniques for thin-film microelectronic circuits (including active devices) on flexible substrates.

BIBLIOGRAPHY

Allan, Roger, "Semiconductor Memories," IEEE Spectrum, August 1975, pp. 40-45.

Altman, Laurence, "LSI Multiplies Design Options," Electronics, October 16, 1975, pp. 110-114.

Altman, Laurence, "Special Report: CMOS Enlarges Its Territory," Electronics, May 15, 1975, pp. 77-88.

"Bipolar, MOS Large-Scale Integration Vie for Spotlight as Device Designers Meet," Electronics Staff, Electronics, November 1975, pp. 97-102.

Blattner, D. J., "Choosing the Right Programs for Computer-Aided-Design," Electronics, April 29, 1976, pp. 102-105.

"Charge-Coupled Devices for Multichannel Video Processors," Air Force Avionics Laboratory Technical Report AFAL-TR-75-104, prepared by Texas Instruments, April 1976.

Crawford, Bob, "Implanting Depletion Devices to Boost MOS Performance," Electronics, April 24, 1972.

"Diagnosing Electronic Ailments," Circuits Manufacturing, June 1975, pp. 44-50.

Dunkley, J. L., Bayazit, Y. N., and Tickle, A. C., Integrated Device Analysis Modeling and Design, Air Force Avionics Laboratory Report AFAL-TR-75-169, September 1975.

Eaton, S. S., "Sapphire Brings Out the Best in MOS," Electronics, June 12, 1975, pp-115-120.

Fogiel, Max, Modern Microelectronics, Research and Education Association, 1972.

Handbook of Thick Film Hybrid Microelectronics, Edited by Charles A. Harper, McGraw Hill Book Company, Inc., 1974.

Handbook of Thin Film Technology, Edited by L. I. Maissel and L. Glang, McGraw Hill Book Company, Inc., 1970.

Hodges, David A., Semiconductor Memories, IEEE Press Book, 1972.

House, Dave, "CCD-vs-RAM for Bulk Storage Applications," Proceedings of the 12th IEEE Computer Society International Conference, February 1976, pp.58-61.

Hybrid Microcircuit Reliability Data, IIT Research Institute, Pergamon Press, 1976.

Keister, F. Z. and Scapple, R. Y., "A Thin-Film Multilayering Technique for Hybrid Microcircuits," Solid State Technology, May 1974, pp 44-47.

Lyman, J., "Film Carriers Win Productivity Prize," Electronics, October 16, 1975, pp. 122-125.

Marcuse, Dietrich, Integrated Optics, IEEE Press Book, 1973.

Mattera, L., "Component Reliability, Part 1: Failure Data Bear Watching," Electronics, October 2, 1975, pp. 91-98.

Mattera, L., "Component Reaiability, Part 2: Hearing from Users and Vendors," Electronics, October 30, 1975, pp. 87-94.

Mattera, L., "Monolithics Mature, Passive Improve," Electronics, October 16, 1975, pp. 116-120.

Mattera, L., "Reliability Revisited: Failure-Rate Comparisons are Given a Second Look," Electronics, December 25, 1975, pp. 83-85.

Proceedings of the 26th Electronic Components Conference, April 1976.

Rodriguez-Corredera, Manual, "Packaging Portable Military Ground Equipment," Electronic Packaging and Production, April 1976, pp. 61-70.

Ronen, R. S. and Micheletti, F. B., "Recent SOS Technology, Advances and Applications," Solid State Technology, August 1975, pp. 39-46.

Scrupski, S. E. "High-Density Bipolars Spur Advances in Computer Design," Electronics, October 30, 1975, pp. 81-86.

Sideris, G., "The LSI Tradeoffs," Space/Aeronautics, March 1969, pp. 64-75.

Surber, W. A., "Optimum Design Procedure for LSI Circuits," Data and Communications Design, November-December 1972, pp. 11-19.

Verhofstadt, P. W. J., "Technology for Microprocessor Hardware," Proceedings of the 12th IEEE Computer Society International Conference, February 1976, pp. 19-22.